CLAIMS

What is claimed is:

1. An electronic device comprising:

a dielectric substrate having a first surface and a second surface, and a via connecting the first and second surface, wherein the via has a horizontal cross sectional area;

a first and a second sacrificial copper structure coupled to the first and the second surface and surrounding the via, respectively, wherein each of the first and second sacrificial copper structures covers an area of no more than three times the horizontal cross sectional area of the via; and

wherein the first and the second sacrificial copper structures are formed on the substrate via a photolithographic process.

2. The electronic device of claim 1 wherein the substrate comprises a wiring board.

3. The electronic device of claim 2 wherein the first and the second surface of the dielectric material comprise a copper layer.

4. The electronic device of claim 1 wherein the via has a via surface, and wherein the via surface comprises copper.

5. The electronic device of claim 4 wherein the copper of the via surface and the first and second sacrificial copper structure are formed in a single process.

6. The electronic device of claim 1 wherein the via has a via diameter, wherein the first and second sacrificial copper structures have a first and second structure diameter, respectively, and wherein at least one of the first and second structure diameters are 150 microns larger than the via diameter.

7. The electronic device of claim 1 further comprising a via fill material disposed within the via.

8. The electronic device of claim 7 wherein the via fill material comprises a resin.

9. The electronic device of claim 7, wherein the via fill material is further disposed on the substrate in an area other than the via, and further comprising a photoresist layer between the first surface and the via fill material.

10. The electronic device of claim 1 wherein each of the first and second sacrificial copper structures covers an area of no more than two times the horizontal cross sectional area of the via.

11. A method of manufacturing an electronic device, comprising:

providing a dielectric substrate with a first surface and a second surface, and forming a via that connects the first and second surface, wherein the via has a horizontal cross sectional area;

forming in a photolithographic process a first and a second sacrificial electrically conductive structure on the first and the second surface and surrounding the via, respectively, wherein each of the first and second sacrificial copper structures covers an area of no more than three times the horizontal cross sectional area of the via; and

filling the via with a via fill material, and removing the first and second sacrificial copper structures.

12. The method of claim 11 wherein at least one of the first and second surfaces further comprise a copper layer.

13. The method of claim 11 wherein the via has a via surface, and wherein the via surface comprises copper.

14. The method of claim 13 wherein the copper of the via surface and the first and second sacrificial copper structure are formed in a single process.

15. The method of claim 11 wherein the via fill material comprises a resin.

16. The method of claim 11 wherein the step of removing the via fill material comprises mechanical abrasion.

17. The method of claim 11 wherein the step of forming the first and second sacrificial copper structures comprises forming a photoresist layer on the first and second surface, respectively, and wherein the photoresist layer is removed prior to the step of removing the first and second sacrificial copper structures.

18. The method of claim 11 wherein each of the first and second sacrificial copper structures covers an area of no more than two times the horizontal cross sectional area of the via.

19. The method of claim 11 wherein the area of the first sacrificial copper structure is different from the area of the second sacrificial copper structure.

20. The method of claim 11 further comprising forming at least one of a nickel layer and a gold layer on the at least one of the first and second surface.